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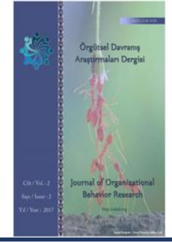

Dimensional Analytical Model for J-TFET

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ABSTRACT

In this study, a 2-D explicit analytical drain current model for junctionless tunneling field effect transistor (J-TFET) is proposed. The potential profile is found by solving the Poisson's equation. From the potential model, the electric field is derived and is utilized to extract the expression for the drain current by analytically integrating the band to band tunneling generation rate over the tunneling region. The proposed model predicts the transfer (I_{DS}-V_{GS}) and the output characteristics (I_{DS}-V_{DS}) of the J-TFET with a good accuracy. The validity of the developed model is examined by 2-D simulation results and quite excellent agreement is achieved.

Keywords: *Analytical model; Poisson's equation; junctionless tunneling field effect transistors (J-TFET); surface potential; 2D TCAD simulation.*

1. Introduction

As the minimum feature size scales below 20 nm, the complementary metal-oxide-semiconductor (CMOS) devices face formidable challenges in terms of increase in packing density and power dissipation [1-3]. Thus the incessant power consumption has become an issue of immediate concern [1-3]. In order to curb the rapidly increasing power consumption, an ideal on-off switching device is required to surpass the subthreshold swing (*SS*) limit of 60 mV/dec with an acceptable off-state leakage current (I_{off}) [4-8].

Tunneling field effect transistors (TFETs) rely on the band-to-band tunneling (BTBT) of electrons. They are thus able to operate as fast switches and exhibit a low off-currents at low supply voltages [4-8]. However, TFETs suffer from several major shortcomings including low on-state current (I_{on}) compared to that in the MOSFET [9-25], inherent ambipolar conduction [24-33], and the requirement of steep source/drain junctions for efficient tunneling [34-36]. Nevertheless abrupt highly doped junctions employing complex high thermal processes are not easy to asses due to the diffusion of dopant atoms [34-36].

Considering the fabrication concerns and the limitation on I_{on}, a novel structure called junctionless TFET (J-TFET) has been proposed [37-39]. In the J-TFET, there is no stringent requirement for precisely steep p-n junction. It utilizes appropriate workfunction for creating the source and drain regions and thus avoids any random dopant fluctuation [40-42]. The J-TFET has shown tremendous potential as it combines advantages of the J-FET with high I_{on}, and TFET with sharp subthreshold slope [40-42].

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Different aspects of the J-TFET have been studied using numerical simulation **[37-42].** However, to the best of our knowledge, there is no analytical model for the J-TFET and thus development of such models are of much interest to the device community. An analytical model will be useful for circuit design and better insight into the performance of the device [**43-51**]. The objective of this work is therefore, to develop an analytical model for the J-TFET.

In this paper, we have proposed a simple and accurate analytical model for the potential, the electric field and the drain current of the J-TFET. First, we calculate the potential profile and the electric field distribution in the source and the channel regions of the J-TFET by solving the 2-D Poisson's equation using Young's parabolic potential approximation. Next, by employing Kane's model, an analytical expression for the drain current is extracted by integrating the BTBT generation rate over the tunneling region. Finally, the analytical model is compared with simulation results.

2. Device Parameters and Simulation Models

Fig. 1 shows schematic cross sectional views of the J-TFET fabricated on a uniform and homogenous n^+ doped material. To realize a P^+-I-N^+ J-TFET structure, two different metals are utilized side by side, denoted as P-Gate (PG) and Main-Gate (MG), where the work function of the PG (ϕ_{PG}= 5.93 eV) is greater than that of the MG (ϕ_{MG}= 4.5 eV). The length of the PG and the MG are L_{PG} and L_{MG}, respectively. While the MG is responsible for turning on the device, the PG is kept at zero voltage in both the off and the on states. t_{ox} and t_{si} are the thickness of gate oxide and silicon body, respectively and ε_{ox} is dielectric constant. The air gap between the PG and the MG is 1 nm. Nevertheless, our model neglects the length of this region.

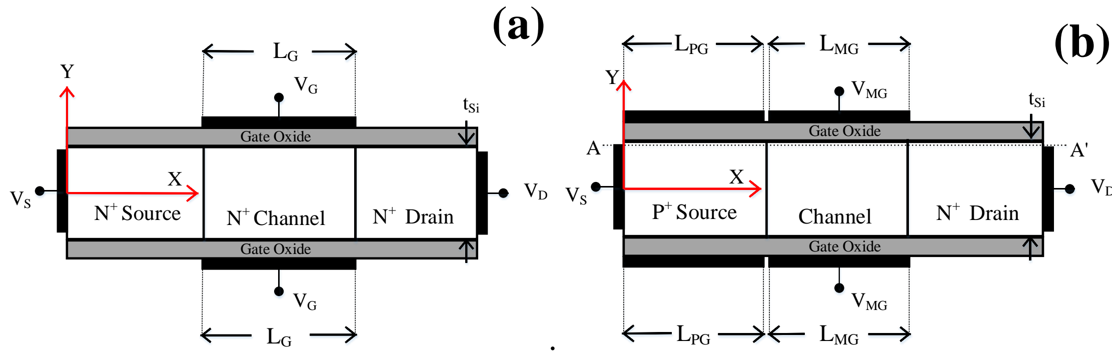


Fig. 1. Cross sectional views of the (a) JT, and (b) J-TFET structures.

3. Model Derivation

3. 1. Potential

The potential is derived by the solution of the 2D Poisson's equation in the silicon thin film:

$$\frac{d^2\Phi_i(x,y)}{dx^2}+\frac{d^2\Phi_i(x,y)}{dy^2}=\frac{-q}{\varepsilon_{si}}N_D$$

for $0 \le x \le L; 0 \le y \le t_{Si}$ (1)

where $\Phi_i(x,y)$ is the potential at any point (x,y), N_D is the doping concentration, assumed to be uniform within the whole silicon thin film and ε_{si} is the dielectric constant of the silicon. It is worth noting that the sum of the L_{PG} and L_{MG} is considered as L, i.e. where the modeling is carried out. The 2D channel potential, $\Phi(x,y)$, can be approximated by a simple parabolic potential as proposed by Young **[43-46]**:

$$\Phi_i(x,y)=a_1(x)+a_2(x)y+a_3(x)y^2 \tag{2}$$

The potential under the PG and MG gates, in the J-TFET structure can be written as:

$$\Phi_{PG}(x,y)=a_{11}(x)+a_{21}(x)y+a_{31}(x)y^2 \quad \text{For } 0 \le x \le L_{PG}; \tag{3}$$

$$\Phi_{MG}(x,y)=a_{12}(x)+a_{22}(x)y+a_{32}(x)y^2 \quad \text{For } L_{PG} \le x \le L_{PG}+L_{MG}; \tag{4}$$

To evaluate $a_1(x)$, $a_2(x)$, and $a_3(x)$, boundary conditions are imposed in y-direction. The following boundary conditions should be satisfied by $\Phi_{PG}(x,y)$:

(1) Because of the symmetry of the channel potential along the y-direction; the electric field at y=0 must be zero under the PG:

$$\left.\frac{\partial\Phi_{PG}(x,y)}{\partial y}\right|_{y=0}=0; \tag{5}$$

(2) Under the PG, the electric flux between the silicon channel and top/bottom gate oxide is continuous:

$$\left.\frac{\partial\Phi_{PG}(x,y)}{\partial y}\right|_{y=\frac{t_{Si}}{2}}=-\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\Phi_{sPG}(x)-(V_{PGs}-V_{fbPG})}{t_{ox}}; \tag{6}$$

where t_{ox} and t_{si} are the thicknesses of the gate oxide and silicon thin film, respectively, ε_{ox} is the dielectric constant of the gate oxide, and $\Phi_{sPG}(x)$ is the surface potential under the PG, V_{PGs} is the PG to source bias voltage which is kept at zero bias. V_{fbPG} represents the flatband voltage of the silicon layer under the PG and is given by:

$$V_{fbPG}=\phi_{PGs}=\phi_{PG}-\phi_{si} \tag{7}$$

with

$$\phi_{si}=\chi+\frac{E_g}{2}-V_t.\log(\frac{N_D}{n_i}) \tag{8}$$

where ϕ_{PG} and ϕ_{si} are the workfunctions of the PG and the silicon, E_g is the bandgap, χ is the electron affinity, V_t is the thermal voltage, and n_i is the intrinsic carrier concentration.

(3) The central potential $\Phi_{cPG}(x,y)$ is a function of x only;

$$\Phi_{cPG}(x) = \Phi_{cPG}(x,0) \tag{9}$$

The surface potential in the silicon layer, $\Phi_{sPG}(x,y)$, is given by;

$$\Phi_{sPG}(x) = \Phi_{PG}(x,y)\Big|_{y=\frac{t_{si}}{2}} = a_{11}(x) + a_{21}(x)\frac{t_{si}}{2} + a_{31}(x)\frac{t_{si}^2}{4} \tag{10}$$

The expressions for the $a_{11}(x)$, $a_{21}(x)$ and $a_{31}(x)$ are then obtained by substituting boundary conditions (5), (6), (9) into equation (3) and (10):

$$a_{11}(x) = \Phi_{cPG}(x); \tag{11}$$

$$a_{21}(x) = 0; \tag{12}$$

$$a_{31}(x) = -\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{si}}\frac{\Phi_{sPG}(x) - (V_{PGs} - V_{fbPG})}{t_{ox}}; \tag{13}$$

The 2D channel potential $\Phi_{PG}(x,y)$ can be achieved, since $a_{11}(x)$, $a_{21}(x)$ and $a_{31}(x)$ are known:

$$\Phi_{PG}(x,y) = \Phi_{cPG}(x) - \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{si}}\frac{\Phi_{sPG}(x) - (V_{PGs} - V_{fbPG})}{t_{ox}}y^2 \tag{14}$$

Here

$$\Phi_{sPG}(x) = \frac{4\Phi_{cPG}(x)\varepsilon_{si}t_{ox} + t_{si}\varepsilon_{ox}(V_{PGs} - V_{fbPG})}{4\varepsilon_{si}t_{ox} + t_{si}\varepsilon_{ox}} \tag{15}$$

By substituting equation (14) and (15) into equation (1), the central potential of the silicon thin film under the PG need to satisfy the following equation:

$$\frac{d^2\Phi_{cPG}(x)}{dx^2} - \frac{1}{\lambda^2}(\Phi_{cPG}(x) - \psi_{PG}) = 0 \tag{16}$$

Where λ is the scaling length.

$$\frac{1}{\lambda^2} = \frac{8\varepsilon_{ox}}{4t_{si}\varepsilon_{si}t_{ox} + \varepsilon_{ox}t_{si}^2}$$

(17)

$$\psi_{PG} = V_{PGs} - \omega_{PG} \quad (18)$$

$$\omega_{PG} = V_{fbPG} + \frac{qN_D t_{si} t_{ox}}{2\varepsilon_{ox}} + \frac{qN_D t_{si}^2}{8\varepsilon_{si}}$$

(19)

The general solution of the ordinary differential equation (16) can be expressed as:

$$\Phi_1(x, y=0) = \Phi_{cPG}(x) = b_1 e^{\frac{1}{\lambda}x} + c_1 e^{-\frac{1}{\lambda}x} + \varphi_{cPG} \qquad 0 \le x \le L_{PG} \quad (20)$$

Also, using the same approach and similar boundary conditions, the potential under the MG is:

$$\Phi_{MG}(x, y) = \Phi_{cMG}(x) - \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{si}} \frac{\Phi_{sMG}(x) - (V_{MGs} - V_{fbMG})}{t_{ox}} y^2$$

(21)

$$\Phi_{sMG}(x) = \frac{4\Phi_{cMG}(x)\varepsilon_{si}t_{ox} + t_{si}\varepsilon_{ox}(V_{MGs} - V_{fbMG})}{4\varepsilon_{si}t_{ox} + t_{si}\varepsilon_{ox}}$$

(22)

$$\frac{d^2\Phi_{cMG}(x)}{dx^2} - \frac{1}{\lambda^2}(\Phi_{cMG}(x) - \psi_{MG}) = 0$$

(23)

$$\psi_{MG} = V_{MGs} - \omega_{MG} \quad (24)$$

$$\omega_{MG} = V_{fbMG} + \frac{qN_D t_{si} t_{ox}}{2\varepsilon_{ox}} + \frac{qN_D t_{si}^2}{8\varepsilon_{si}}$$

(25)

V_{fbMG} represents the flatband voltage for the silicon thin film under the MG:

$$V_{fbMG} = \phi_{MGs} = \phi_{MG} - \phi_{si} \quad (26)$$

where ϕ_{MG} and ϕ_{si} are the workfunctions of the MG and silicon, respectively. Thus, we can easily achieve the expression for the $\Phi_{cMG}(x,y)$ as:

$$\Phi_{MG}(x, y=0) = \Phi_{cMG}(x) = b_2 e^{\frac{1}{\lambda}x} + c_2 e^{-\frac{1}{\lambda}x} + \varphi_{cMG} \qquad L_{PG} \leq x \leq L_{PG} + L_{MG} \quad (27)$$

The coefficients b_1, b_2, c_1 and c_2 can be obtained by the following boundary conditions:

(1) The potential at the source end is zero;

$$\Phi_{cPG}(x=0) = 0 \quad (28)$$

(2) The potential at the interface of the two dissimilar gate materials is continuous;

$$\Phi_{cPG}(x=L_{PG}) = \Phi_{cMG}(x=L_{PG}) \quad (29)$$

(3) The electric flux at the interface of the two dissimilar gate materials is continuous;

$$\frac{d\Phi_{cPG}(x)}{dx}\bigg|_{x=L_{PG}} = \frac{d\Phi_{cMG}(x)}{dx}\bigg|_{x=L_{PG}} \quad (30)$$

(4) The potential at the drain end is V_{ds};

$$\Phi_{cMG}(x)\Big|_{x=L_{PG}+L_{MG}} = V_{ds} \quad (31)$$

The coefficients a_1, a_2, b_1, and b_2 can be obtained by using the previously mentioned boundary conditions:

$$b_1 = \frac{e^{-\frac{L}{\lambda}}\psi_{PG} + V_{ds} - \psi_{MG} + (\psi_{MG} - \psi_{PG})\cosh(\frac{L_{MG}}{\lambda})}{2\sinh(\frac{L}{\lambda})} \quad (32)$$

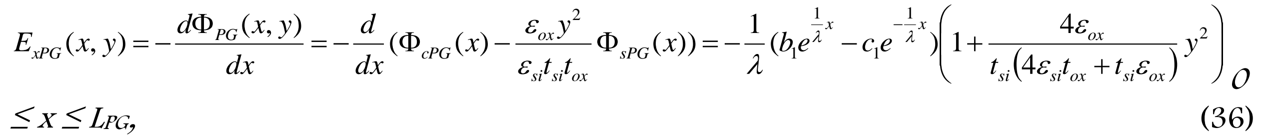
$$b_2 = \frac{e^{-\frac{L}{\lambda}}\psi_{PG} + V_{ds} - \psi_{MG} + (\psi_{MG} - \psi_{PG})\cosh(\frac{L_{PG}}{\lambda})e^{-\frac{L}{\lambda}}}{2\sinh(\frac{L}{\lambda})} \quad (33)$$

$$c_1 = \frac{-e^{-\frac{L}{\lambda}}\psi_{PG} - V_{ds} + \psi_{MG} - (\psi_{MG} - \psi_{PG})\cosh(\frac{L_{MG}}{\lambda})}{2\sinh(\frac{L}{\lambda})} \quad (34)$$

$$c_2 = \frac{-e^{\frac{L}{\lambda}}\psi_{PG} - V_{ds} + \psi_{MG} - (\psi_{MG} - \psi_{PG})\cosh(\frac{L_{PG}}{\lambda})e^{\frac{L}{\lambda}}}{2\sinh(\frac{L}{\lambda})} \quad (35)$$

3. 2. Electric Field

The electric field distribution along the channel length can be obtained by differentiating the surface potential. The lateral and vertical electric field can be written by using equation (14), (15), (20), (21), (22), and (27):



$$E_{xPG}(x,y) = -\frac{d\Phi_{PG}(x,y)}{dx} = -\frac{d}{dx}(\Phi_{cPG}(x) - \frac{\varepsilon_{ox}y^2}{\varepsilon_{si}t_{si}t_{ox}}\Phi_{sPG}(x)) = -\frac{1}{\lambda}(b_1e^{\frac{1}{\lambda}x} - c_1e^{-\frac{1}{\lambda}x})\left(1 + \frac{4\varepsilon_{ox}}{t_{si}(4\varepsilon_{si}t_{ox} + t_{si}\varepsilon_{ox})}y^2\right) \quad 0 \le x \le L_{PG}, \quad (36)$$

$$E_{xMG}(x,y) = -\frac{d\Phi_{MG}(x,y)}{dx} = -\frac{d}{dx}(\Phi_{cMG}(x) - \frac{\varepsilon_{ox}y^2}{\varepsilon_{si}t_{si}t_{ox}}\Phi_{sMG}(x)) = -\frac{1}{\lambda}(b_2e^{\frac{1}{\lambda}x} - c_2e^{-\frac{1}{\lambda}x})\left(1 + \frac{4\varepsilon_{ox}}{t_{si}(4\varepsilon_{si}t_{ox} + t_{si}\varepsilon_{ox})}y^2\right) \quad L_{PG} \le x \le L_{PG} + L_{MG}, \quad (37)$$

$$E_{yPG}(x,y) = -\frac{d\Phi_{PG}(x,y)}{dy} = 2\frac{\varepsilon_{ox}y}{4\varepsilon_{si}t_{ox} + \varepsilon_{ox}t_{si}}\left[\frac{4}{t_{si}}\left(b_1e^{\frac{1}{\lambda}x} + c_1e^{-\frac{1}{\lambda}x}\right) + \frac{\varepsilon_{ox}}{t_{ox}\varepsilon_{si}}(V_{PGs} - V_{fbPG})\right] + 2y\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{si}t_{ox}}(V_{PGs} - V_{fbPG}) \quad 0 \le x \le L_{PG}, \quad (38)$$

$$E_{yMG}(x,y) = -\frac{d\Phi_{MG}(x,y)}{dy} = 2\frac{\varepsilon_{ox}y}{4\varepsilon_{si}t_{ox} + \varepsilon_{ox}t_{si}}\left[\frac{4}{t_{si}}\left(b_2e^{\frac{1}{\lambda}x} + c_2e^{-\frac{1}{\lambda}x}\right) + \frac{\varepsilon_{ox}}{t_{ox}\varepsilon_{si}}(V_{MGs} - V_{fbMG})\right] + 2y\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{si}t_{ox}}(V_{MGs} - V_{fbMG}) \quad L_{PG} \le x \le L_{PG} + L_{MG}, \quad (39)$$

Thus, the overall effective electric field under the PG and MG is given by:

$$E_{PG} = \sqrt{E_{xPG}^2 + E_{yPG}^2} \quad (40)$$

$$E_{MG} = \sqrt{E_{xMG}^2 + E_{yMG}^2} \quad (41)$$

3. 3. Drain Current

In this section, we will drive an analytical expression for drain current. It is well known that the current of a TFET is dependent on the BTBT probability **[4-8]**. The most widely used and well-established model to calculate the tunneling current is the Kane's model **[43-51]**, which determines the effective BTBT generation rate for the carrier tunneling from the source valence band into the channel conduction band:

$$G_{BTBT} = A\frac{E^D}{E_g^{1/2}}\exp(-B\frac{E_g^{3/2}}{E}) \qquad (42)$$

Where E is the electric field; D is 2.5 for indirect and 2 for the direct tunneling processes; A and B are the tunneling process-dependent parameters and are equal to 3.5×10^{21} $eV^{1/2}$/cm s V^2 and 22.5×10^6 V/cm $eV^{3/2}$ for silicon as given in **[53-54]**. By integrating G_{BTBT} along the tunneling path (lateral direction) and over the entire channel thickness, the drain current per unit width (A/µm) can be computed as **[43-51]**:

$$I_D = q\iint G_{BTBT}dxdy \qquad (43)$$

Thus by substituting (42) into (43), the drain current can be written as:

$$I_D = q\int_{x_1}^{x_2}\int_{y_1=-\frac{t_{si}}{2}}^{y_2=\frac{t_{si}}{2}}(A\frac{E^D}{E_g^{1/2}}\exp(-B\frac{E_g^{3/2}}{E}))dxdy \qquad (44)$$

It is well known that the effective probability of carrier tunneling is dependent on the amount of the electric field which in turn is a function of the tunneling path length (l_{path}). As can be seen from **Fig. 2**, l_{path} varies from l_1 to l_2, thus l_{path} ranges between x_1 and x_2 **[46, 50]**. Note that x_1 and x_2 both lie under the MG. Thus, it is reasonable to consider E in (44), to be equal to E_{MG}. Also note that, the limit of integration along x direction is $l_1=x_1$ and $l_2=x_2$, i.e. the tunneling window across which carriers tunnel through.

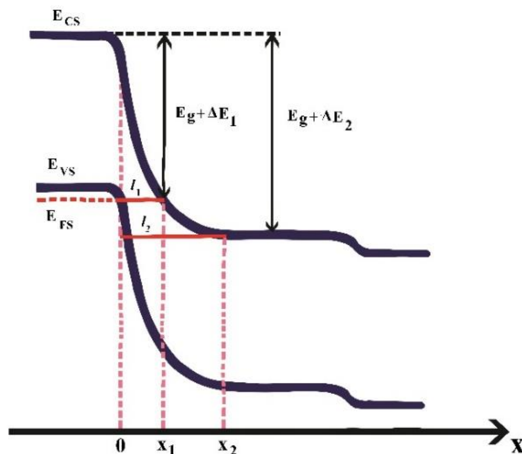


Fig. 2. Energy band diagram along the x-direction during on-state of the J-TFET. It illustrates the effective electrons tunneling at the source-channel junction.

Fig. 2 depicts that the tunneling of carriers from source valence band into the channel conduction band starts at $x = x_1$. At this point, the channel potential reaches $(E_g+\Delta E_1)/q$. E_g is the bandgap of the silicon and $\Delta E_1 = E_{VS}-E_{FS}$ is the difference between source valence band and Fermi level. By using (22) and (27), x_1 can be obtained from:

$$\phi_{s2}(x)\Big|_{x=x_1} = \frac{E_g + \Delta E_1}{q} \qquad (45)$$

Similarly, at $x = x_2$, when the channel potential reaches $(E_g+\Delta E_2)/q$, carriers stop tunneling from the source valence band into the channel conduction band. Here, $\Delta E_2 = E_{VS}-E_{CC}$ is the difference between the source valence band and the channel conduction band. Hence, to evaluate x_2, we utilize (22), and (27) as follows:

$$\phi_{s2}(x)\Big|_{x=x_2} = \frac{E_g + \Delta E_2}{q} \qquad (46)$$

4. Model Validation

In this section we will validate our proposed model by comparing it with the 2D TCAD simulation results. We evaluate the efficacy of the model by varying some important parameters which are listed in each figure.

Fig. 3 compares the surface potential at different V_{GS} and MG workfunctions for the proposed model and device simulation results. The V_{DS} is set to be 1.0 V. As shown in **Fig. 3**, employing positive bias on V_{GS}, and also lower MG workfunction push down the conduction and valence band energy levels in the channel. This highly influences the tunneling current. Meanwhile the band energy levels under the PG remain at higher energies due its large workfunction. Thus further increase in V_{GS}, enhances the channel potential and pins the channel potential to the drain potential. However the potential is at its minimum value under the PG due to the PG's large workfunction. Thanks to the different workfunctions of the PG and the MG, the surface potential changes sharply at the PG/ MG interface. It is quite clear from **Fig. 3** that the model is tracking the potential with good accuracy.

Fig. 4 shows the electric field within the J-TFET's silicon thin film as a function of V_{GS}. A peak in the electric field appears near the source-channel interface (at the interface of the PG and the MG) because of the step potential profile (**Fig. 3(a)**). In the on-state, as the V_{GS} is increased, the height of this peak is enlarged. This can further accelerate the electrons in the channel, improve the efficiency of carrier transport and increase the tunneling current. On the other hand, the lower electric field at the drain end helps to mitigate the problems associated with the I_{off} and I_{amb} in the J-TFET. It is clear form **Fig. 4** that our analytical model closely approximates the simulation results.

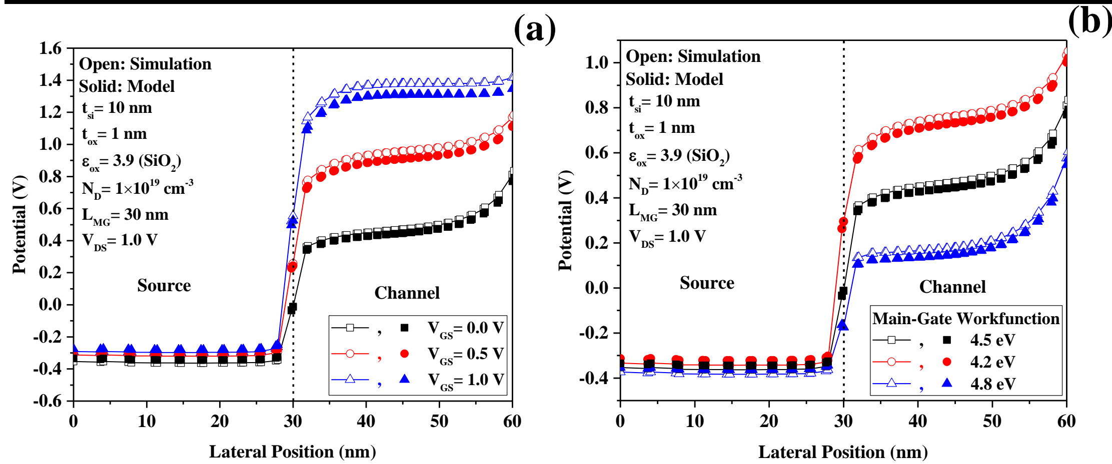


Fig. 3. The potential distribution along lateral position for the proposed model (solid symbols) and its comparison with simulation results (open symbols) for different (a) gate voltages and (b) workfunction of the Main-Gate.

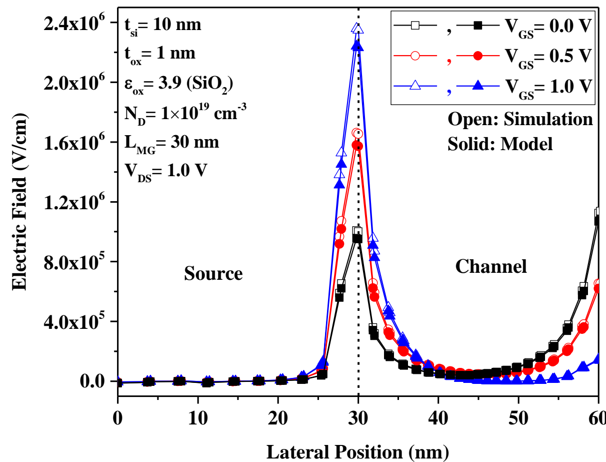


Fig. 4. The electric field distribution along lateral position for the proposed model (solid symbols) and its comparison with simulation results (open symbols) for various gate voltages.

Fig. 5 compares the J-TFET's transfer characteristics (I_{DS}- V_{GS}) and surface potential for various doping density of the silicon thin film. As shown in this figure, the model and simulation results are in close agreement. Lower doping concentration of the silicon film can be used to exert more effective control on the channel potential by the gate bias. Thus as the doping concentration of the silicon film steadily increases, the surface potential is pulled up, leading to a weaker control of the gate. Also, as shown in **Fig. 5 (b)**, the I_{on} enhances with increase while the I_{off} reduces with decrease in the doping density of the silicon film. Thus, reducing the doping concentration of the silicon thin film is an appropriate means for suppressing the I_{off}.

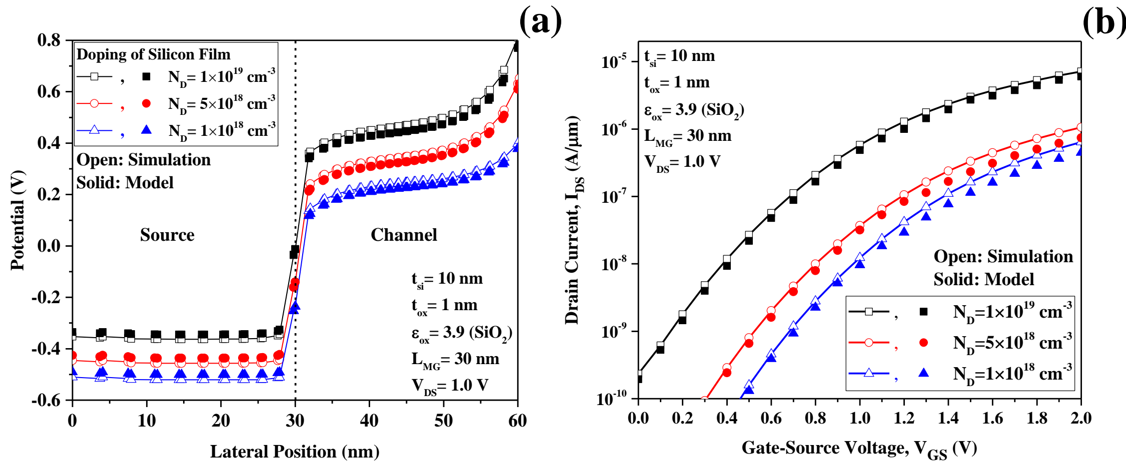


Fig. 5. (a) Lateral potential distribution and (b) transfer characteristics (I_{DS}- V_{GS}) for the proposed model (solid symbols) and its comparison with simulation results (open symbols) for different doping concentration of the silicon film.

Fig. 6 (a) demonstrates the J-TFET's transfer characteristics (I_{DS}- V_{GS}) with V_{DS} as a parameter. As expected, current saturates at higher V_{GS}. It is clear from this figure that when the V_{DS} is increased, the drain current is enhanced. Also, in **Fig. 6 (b)**, the J-TFET's output characteristics (I_{DS}- V_{DS}) are shown for 1.4 V < V_{GS}< 1.6 V. We observe that the structure clearly exhibits an exponential region as well as a saturation region of operation. The saturation region in the I_{DS}- V_{DS} is due to the progressively less dependence of the tunneling width on V_{DS} as this voltage is increased.

A large variation in current as the gate voltage varies, proves the good control of the gate on the channel. When a low gate voltage is applied, the tunneling barrier is still high and hence the probability of the carrier tunneling is small. Upon applying higher gate voltages, improvement in I_{on} is observed. This is attributed to the reduction in the tunneling barrier width which in turn enhances the carrier tunneling probability. As numerical integration of the BTBT has been carried out over the entire device structure rather than using a single tunneling path, the model is able to accurately predict both the transfer as well as the output characteristics.

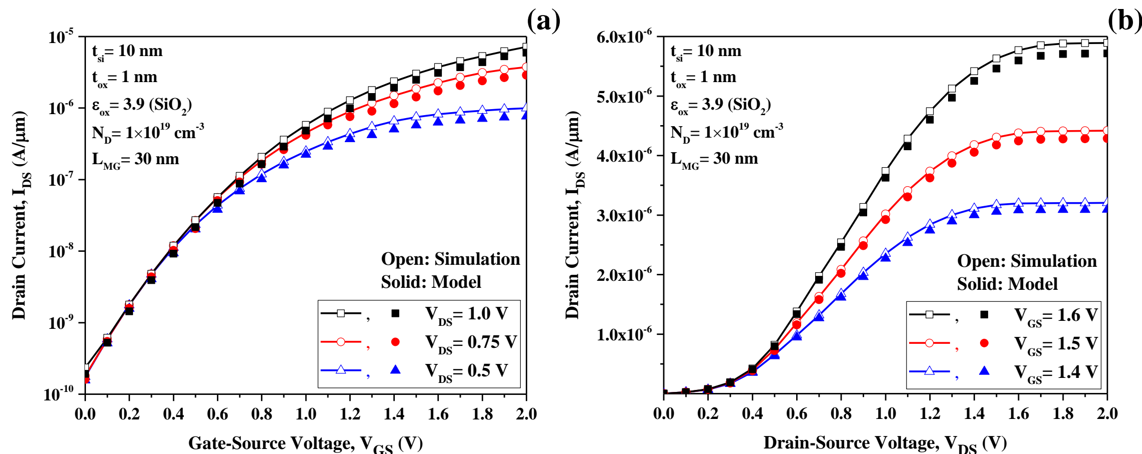


Fig. 6. (a) The transfer characteristics (I_{DS}- V_{GS}) and the output characteristics (I_{DS}- V_{DS}) for the proposed model (solid symbols) and its comparison with simulation results (open symbols).

5. Conclusion

In conclusion, using "Young's parabolic potential approximation", we have derived an analytical model for calculation of the potential, electric field and drain current of the J-TFET. The comparison of the data obtained using present model with those obtained by TCAD simulation results confirms the accuracy of our model. The model takes into account the influences of the structural parameters, and it accurately predicts the electrostatic potential and drain current behavior over a large number of the design parameters including silicon thin film doping concentration (N_D), gate and drain voltages as well as the workfunction of the MG. The proposed analytical model not only provides guidance for the design and application of the J-TFETs, but also lay a theoretical foundation for further research.

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Conflict of Interest:

Funding:

Ethical statements:

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